PENDING CLAIMS

The following is a complete list of claims currently pending in the application. Please cancel claims 20-22, 27. 30-31, 34 and 39. Please amend claims 26, 36-38, and 40 as shown below.

1-2. (Cancelled)

3. (Previously amended) A method for making a transistor containing a gate dielectric structure, comprising:

providing a gate conductor;

providing a channel; and

providing, between the gate conductor and the channel, an oxide layer of the gate dielectric structure by an in-situ steam generation process, wherein the transistor is a thin film transistor.

4. (Cancelled)

5. (Previously amended) The method of claim 3, wherein the in-situ steam generation process is performed at a temperature ranging from about 600 to about 900 degrees Celsius.

6. (Previously amended) The method of claim 3, wherein the in-situ steam generation process is performed at a pressure ranging from about 100 millitorr to about 760 torr.

7. (Previously amended) The method of claim 3, wherein the in-situ steam generation process is performed for a time sufficient to deposit an oxide thickness of about 10 to about 200 angstroms.

8. (Previously amended) The method of claim 28, further including annealing the oxide layer in a nitric oxide atmosphere.

9. (Previously amended) A method for making a SONOS device, comprising:

providing a channel region;

providing a first oxide layer on the channel region by an in-situ steam generation process;

providing a nitride layer on the first oxide layer; and

providing a second oxide layer on the nitride layer, wherein the device is a SONOS device.

10-11. (Cancelled)

12. (Original) The method of claim 9, wherein the in-situ steam generation process is performed at a temperature ranging from about 750 to about 1050 degrees Celsius.

13. (Original) The method of claim 9, wherein the in-situ steam generation process is performed at a pressure ranging from about 100 millitorr to about 760 torr.

14. (Original) The method of claim 9, wherein the in-situ steam generation process is performed for a time sufficient to deposit an oxide thickness of about 10 to about 200 angstroms.

15. (Original) The method of claim 9, further including annealing the oxide layer in a nitric oxide atmosphere.

16-22. (Cancelled)

23. (Previously amended) A thin film transistor containing a gate dielectric structure made by a method comprising:

providing a gate conductor;

providing a channel region; and

providing, between the gate conductor and the channel region, an oxide layer of the gate dielectric structure on the channel region by an in-situ steam generation process, wherein the transistor is a thin film transistor.

24. (Previously amended) A SONOS semiconductor device made by a method comprising:

providing a channel region;

providing a first oxide layer on the channel region by an in-situ steam generation process;

providing a nitride layer on the first oxide layer; and

providing a second oxide layer on the nitride layer wherein the device is a SONOS semiconductor device.

25. (Previously amended) An integrated circuit containing a thin film transistor with a gate dielectric structure made by a method comprising:

providing a gate conductor;

providing a channel; and

providing, between the gate conductor and the channel, an oxide layer of the gate dielectric structure by an in-situ steam generation process wherein the transistor is a thin film transistor.

26. (Currently amended) An integrated circuit containing a SONOS semiconductor device made by a method comprising:

providing a ~~silicon wafer or silicon~~ polysilicon layer;

providing a first oxide layer on the ~~silicon wafer or silicon~~ polysilicon layer by an in-situ steam generation process;

providing a nitride layer on the first oxide layer; and

providing a second oxide layer on the nitride layer wherein the device is a SONOS semiconductor device.

27. (Cancelled)

28. (Previously added) The method of claim 3, wherein the transistor is a SONOS transistor.

29. (Previously added) The method of claim 3, wherein the transistor comprises a floating gate.

30-31. (Cancelled)

32. (Previously added) The transistor of claim 23, wherein the transistor comprises a floating gate.

33. (Previously added) The integrated circuit of claim 25, wherein the transistor comprises a floating gate.

34-35. (Cancelled)

36. (Currently amended) A method for making a SONOS device, comprising:

providing a polysilicon channel region;

providing a first oxide layer in contact with the polysilicon channel region by an in-situ steam generation process;

providing a nitride layer in contact with the first oxide layer; and

providing a second oxide layer in contact with the nitride layer.

37. (Currently amended) A SONOS semiconductor device made by a method comprising:

providing a polysilicon channel region;

providing a first oxide layer in contact with the polysilicon channel region by an in-situ steam generation process;

providing a nitride layer in contact with the first oxide layer; and

providing a second oxide layer in contact with the nitride layer.

38. (Currently amended) An integrated circuit containing a SONOS semiconductor device made by a method comprising:

providing a ~~silicon wafer or silicon~~ polysilicon layer;

providing a first oxide layer in contact with the ~~silicon wafer or silicon~~ polysilicon layer by an in-situ steam generation process;

providing a nitride layer in contact with the first oxide layer; and

providing a second oxide layer in contact with the nitride layer, wherein the device is a SONOS semiconductor device.

39. (Cancelled)

40. (Currently amended) A method for making a gate dielectric structure for a thin film transistor ~~or a SONOS device~~, comprising:

providing a gate conductor;

providing a channel region; and

providing, between the gate conductor and the channel region and in contact with the channel region, an oxide layer of a gate dielectric structure by an in-situ steam generation process performed at a temperature ranging from about 600 to about 1050 degrees Celsius, a pressure ranging from about 100 millitorr to about 760 torr, and for a time sufficient to deposit an oxide thickness of about 10 to about 200 angstroms, wherein the gate dielectric structure is for a thin film transistor ~~or a SONOS device~~.

41. (Previously amended) A thin film transistor containing a gate dielectric structure made by a method comprising:

providing a gate conductor;

providing a channel region; and

providing, between the gate conductor and the channel region and in contact with the channel region, an oxide layer of the gate dielectric structure on the channel region by an in-situ steam generation process, wherein the transistor is a thin film transistor.

42. (Previously amended) An integrated circuit containing a thin film transistor with a gate dielectric structure made by a method comprising:

providing a gate conductor;

providing a channel; and

providing, between the gate conductor and the channel and in contact with the channel, an oxide layer of the gate dielectric structure by an in-situ steam generation process, wherein the transistor is a thin film transistor.

CLAIM AMENDMENTS

Claims 26, 36-38, and 40 are amended in this response. None of these amendments introduces new matter.

Claim 26 has been amended to recite an integrated circuit containing a SONOS semiconductor device made by a method comprising providing a polysilicon layer; providing a first oxide layer on the polysilicon layer by an in-situ steam generation process; providing a nitride layer on the first oxide layer; and providing a second oxide layer on the nitride layer wherein the device is a SONOS semiconductor device. The amendments to claim 36-38 similarly specify that the silicon layer or channel region upon which an oxide layer is grown by an in-situ steam generation process is of polysilicon.

Support for these amendments is found in the specification at paragraphs 20 and 37, *inter alia*.

Claim 40 recites a method for making a gate dielectric structure for a thin film transistor, comprising providing a gate conductor; providing a channel region; and providing, between the gate conductor and the channel region and in contact with the channel region, an oxide layer of a gate dielectric structure by an in-situ steam generation process performed at a temperature ranging from about 600 to about 1050 degrees Celsius, a pressure ranging from about 100 millitorr to about 760 torr, and for a time sufficient to deposit an oxide thickness of about 10 to about 200 angstroms, wherein the gate dielectric structure is for a thin film transistor. The prior version of the claim recited a method for making a gate dielectric structure for a thin film transistor *or a SONOS device*. Clearly, this amendment does not add new matter.